WHAT IS CLAIMED AND DESIRED TO BE SECURED BY LETTERS PATENT OF THE UNITED STATES IS:

1. A method for synthesizing an integrated circuit design, the method comprising:

performing physical optimization of block and wire placement, before performing logic synthesis;

partitioning the blocks into cores and shells;

synthesizing the shells and cores; and

recombining the cores and shells into blocks.

2. The method of Claim 1, wherein performing physical optimization of block placement comprises estimating an area of each block.

3. The method of Claim 2, wherein performing physical optimization of wire placement comprises determining a pin assignment layout.

4. The method of Claim 3, wherein performing physical optimization of wire placement further comprises selecting a layer for each wire based on wire length.

5. The method of Claim 4, wherein performing physical optimization of wire placement further comprises minimizing a delay in each wire by inserting buffers at optimal distances.

6. The method of Claim 5, wherein synthesizing the shells comprises determining a proportion of time to assign to each shell on each side of a wire.

7. The method of Claim 5, wherein after synthesizing the shells, the process of performing physical optimization of blocks and wires and partitioning the blocks is incrementally repeated if the wire delays are too long for shell synthesis.

8. A method for designing deep sub-micron integrated circuits, the method comprising:

performing layout of physical blocks by estimating an area for each block;

connecting pins of the blocks with no timing constraints;

assigning each wire to a metal layer pair;

optimizing the speed of each wire for its respective layer;

partitioning the blocks into cores and shells;

synthesizing the shells;

synthesizing the cores; and

recombining the shells and cores.

9. The method of Claim 8, wherein each wire is assigned to a metal layer based on a relative length of the wire.

10. The method of Claim 9, wherein optimizing the speed of each wire comprises minimizing a delay in each wire by inserting buffers at optimal distances.

11. The method of Claim 10, wherein synthesizing the shells comprises determining a proportion of time to assign to each shell on each side of a wire.

12. The method of Claim 11, wherein after synthesizing the shells, the layout procedure is incrementally repeated if the wire delays are too long for shell synthesis.

13. A method for reducing design cycle time for integrated circuits, the method comprising:

laying out blocks by estimating an area for each block;

minimizing a delay in each global wire;

partitioning each block into a core and a shell;

performing logic synthesis an each shell by utilizing a known delay for each wire;

performing logic synthesis on each core; and

recombining the shells and cores.

14. The method of Claim 13, wherein minimizing a delay in each global wire comprises assigning each wire to a layer, and inserting buffers at optimal distances.

15. The method of Claim 14, wherein performing logic synthesis on each shell comprises determining a proportion of time to assign to each shell on each side of a wire.

16. The method of Claim 15, wherein after synthesizing the shells, the layout procedure is incrementally repeated if the wire delays are too long for shell synthesis.

17. A computer readable media, having instructions stored thereon that, when loaded into a computer, cause the computer to perform the steps of:

performing physical optimization of block and wire placement, before performing logic synthesis;

partitioning the blocks into cores and shells;

synthesizing the shells and cores; and

recombining the cores and shells into blocks.

18. The computer readable media according to Claim 17, wherein said steps further comprise:

performing physical optimization of block placement comprises estimating an area of each block.

19. The computer readable media according to Claim 18, wherein said step of performing physical optimization of wire placement comprises determining a pin assignment layout.

20. The computer readable media according to Claim 19, wherein said step of performing physical optimization further comprises selecting a layer for each wire based on wire length.

21. The method of Claim 20, wherein said step of performing physical optimization of wire placement further comprises minimizing a delay in each wire by inserting buffers at optimal distances.

22. The method of Claim 21, wherein said step of synthesizing the shells comprises determining a proportion of time to assign to each shell on each side of a wire.

23. The method of Claim 21, wherein after synthesizing the shells, the process of performing physical optimization of

blocks and wires and partitioning the blocks is incrementally repeated if the wire delays are too long for shell synthesis